6P 18701 (3)

Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 469 553 A1**

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: 91112804.9

(22) Date of filing: 30.07.91

(51) Int. Cl.5: G11B 7/085, G11B 7/08, G11B 7/09

(30) Priority: 30.07.90 JP 201839/90

(43) Date of publication of application: 05.02.92 Bulletin 92/06

(84) Designated Contracting States: DE FR GB

(71) Applicant: NEC CORPORATION
7-1, Shiba 5-chome Minato-ku
Tokyo 108-01(JP)

(72) Inventor: Tomimitsu, Yasuharu
c/o NEC Corporation, 7-1, Shiba 5-chome
Minato-ku, Tokyo(JP)

(74) Representative: Betten & Resch
Reichenbachstrasse 19
W-8000 München 5(DE)

(54) **Disk controller including format control unit instructing directly jump back operation.**

(57) A disk controller for a disk having spirally formed tracks comprises a buffer memory for temporarily storing write data to be recorded on said disk and read data derived from said disk, a first register for temporarily storing current sector information representative of a sector currently accessible, said current sector information being changed in accordance with rotation of said disk, a second register for temporarily storing target sector information representative of a sector from which a data read/write operation starts, comparator means for comparing said current sector information with said target sector information to produce a comparison output signal taking an active level when said current sector information coincides with said target sector information, means for producing a ready signal taking an active level when said write data is stored in said buffer memory or when said buffer memory has a vacancy for accepting said read data, and control means responsive to said comparison output signal and said ready signal for generating a jump back signal when said ready signal is at an inactive level at a time when said comparison output signal takes said active level, said control means further generating, after said comparison signal takes said active level, said jump back signal when said ready signal is at said inactive level at a time when said current sector information changes.

EP 0 469 553 A1

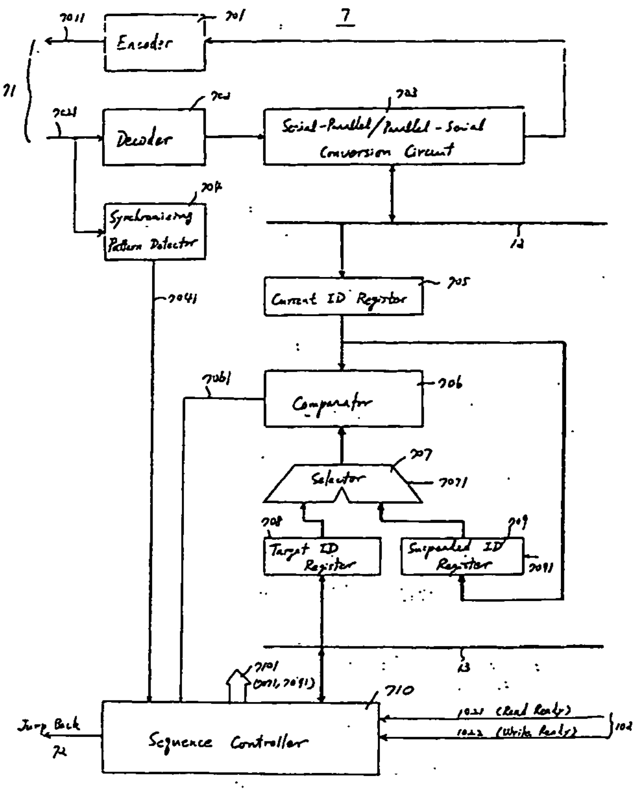

7
Encoder
Decoder
Serial-Parallel/Parallel-Serial Conversion Circuit
Synchronizing Pattern Detector
Current ID Register
Comparator
Selector
Target ID Register
Suspended ID Register
Sequence Controller
Jump Back
(Read Ready)
(Write Ready)

Fig. 2

BACKGROUND OF THE INVENTION

The present invention relates to a disk controller and, more particularly, to an optical disk controller for an optical disk having a spirally formed track.

An optical disk is employed as one of data storage units in an information processing system. An optical disk controller performs a data transfer operation between the disk and a host processor.

The optical disk controller includes in general a buffer memory for temporarily storing write data from the host processor and read data from the disk, a format control unit for converting the write data from the buffer memory into data to be recorded on the disk and the data reproduced from the disk into the read data, and a system controller for responding to commands from the host processor to control the data transfer flow. Further included in the disk controller are a servo controller for controlling the focus and tracking of an optical beam on the disk and a drive controller for ordering, under the control of the system controller, the servo controller to perform a seek operation in which the optical beam moves in random to a target track and a jump operation in which the optical beam jumps to the adjacent track.

When the system controller receives a data transfer command from the host processor, it requests the seek operation of the drive controller, so that the optical beam moves rapidly to the target track. At a time when a target sector on that track is searched, the format controller starts to operate in a data write mode to record the write data from the buffer memory on the disk and in a data read mode to supply the buffer memory with the read data responsive to the data recorded on the disk. It is of course that in the data write mode the write data is transferred from the host processor to the buffer memory and in the data read mode the read data is transferred from the buffer memory to the host processor. Thus, the data transfer is executed between the disk and the host processor.

However, such cases sometimes occur that no write data has been transferred to the buffer memory at a time the target sector is searched and that the write data transfer to the buffer memory is suspended during the data record on the disk. Also in the data read mode, the buffer memory is often fulled with the read data which are not transferred to the host processor yet. In such cases, the data read/write operation is of course suspended until the write data arrives in the buffer memory or until the buffer memory has a vacancy for accepting the read data. On the other hand, the disk continues to rotate. Since the track on the disk is formed spirally, therefore, the accessible sector advances in sequence, so that the target sector is not searched again even when the write data is transferred to the buffer memory or the vacancy for the read data is formed in the buffer memory.

Therefore, the format controller informs the system controller of a fact that the data read/write operation is suspended due to the above reason. In response thereto, the system controller requests the jump operation of the drive controller to back the optical beam up by one track. To back the optical beam up is called hereinafter "jump back".

However, this jump back operation is performed after the response time of the system controller and the drive controller has elapsed, resulting in lowering in an access speed. Moreover, the system controller must be designed to handle the request from the format controller, and hence the load thereof is made large.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide an improved disk controller.

Another object of the present invention is to provide a disk controller which can prevents lowering in an access speed even when a data read/write operation is suspended.

Still another object of the present invention is to provide a disk controller which can achieve a jump back processing operation without making a load of a system controller large.

A disk controller according to the present invention is characterized in that a format control unit generates directly a jump back signal and a servo controller responds directly to that signal to perform a jump back operation.

More specifically, the format control unit comprises a first register for temporarily storing current sector information which indicates a currently accessible sector on a disk and is changed in accordance with the lotation of the disk, a second register for temporarily storing target sector information indicative of a target sector from which a data read/write operation starts, comparator means for comparing the information stored in the first register with the information stored in the second register to produce a comparison output signal taking an active level when the former information coincides with the latter information, and a sequence controller receiving the comparison output signal and a ready signal which takes an active level when write data is already stored in a buffer memory or when the buffer memory has a vacancy for accepting read data and generating the jump back signal when the ready signal is in an inactive level when the comparison output signal takes the active level, the sequence controller further generating, after the comparison output signal takes the active level, the jump back signal when the ready signal is in the

inactive level when the information stored in the first register is changed.

Thus, the format control unit initiates the jump back operation to prevent lowering in an access speed due to the delay of system and drive controllers.

When the sequence controller generates the jump back signal, the sector information at that time is temporarily retained, and the comparator means thereafter compares the current sector information with the retained sector information. The generation of the jump back signal is then controlled in response to the comparison output signal and the ready signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

Fig. 1 is block diagram of a system employing a disk controller according to an embodiment of the present invention;

Fig. 2 is a block diagram representative of a format control unit shown in Fig. 1;

Fig. 3 is a block diagram representative of respective parts of an optical head circuit and a servo controller shown in Fig. 1;

Fig. 4 is a diagram representative of a spiral track on an optical disk;

Fig. 5 is a block diagram representative of a format control unit according to another embodiment of the present invention; and

Fig. 6 is a block diagram representative of respective parts of an optical head circuit and a servo controller corresponding to the format control unit shown in Fig. 5.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to Fig. 1, an optical disk controller according to an embodiment of the present invention includes an interface circuit 8 which receives and supplies commands and data from and to a host processor 14 via a system bus 15. The commands such as a data write command and a data read command from the host processor 14 are supplied to a system controller 11 via a controller bus 13. The system controller 11 responds to the commands thus supplied and calculates ID (Identification) information indicative of a physical address of a sector from which a data read/write operation starts and the number of sectors to be subjected to the data read/write and further generates seek information for moving rapidly an optical beam 31 to a target track on an optical disk 1. The seek information is supplied via a bus 110 to a drive controller 6, whereas read/write command information is supplied via a bus 13 to a format control unit 7 and a memory control unit 10. The data to be written into the disk 1, i.e. write data from the host processor 14, are temporarily stored into a buffer memory 9 through the interface circuit 8 and an internal bus 12. The buffer memory 9 is of a FIFO (first-in first-out) type. The data to be transferred to the host processor 14, i.e. read data derived from the disk 1, are also temporarily stored into the buffer memory 9 and then transferred to the host processor 14 through the interface circuit 9 and the system bus 15. The memory control unit 10 manages the buffer memory 9 through a control line 101 and thus detects the presence/absence of the write data into the memory 9 and the presence/absence of a vacancy for the read data in the memory 9. The detection output is outputted as ready information 102.

On the other hand, the disk 1 is rotated by a spindle motor 2 and the data read/write is carried out by an optical beam 31 from an optical head circuit 3. This circuit 3 produces focus and tracking information 32 for the beam 31, which information is in turn supplied to a servo controller 5. In response thereto, the controller 5 performs the rotation speed control of the motor 2 and the focus and tracking control of the beam 31 through control data 51 and 52. The servo controller 5 is further supplied with a seek control information and track jump information 61 from a drive controller 6. In response thereto, the servo controller 5 opens the servo control loop to move the beam 31 as the seek operation and the track jump operation.

The optical head circuit 3 communicates via a data line 71 with the format control unit with respect to data to be recorded on the disk 1 and data reproduced from the disk 1. The format control unit 7 receives the write data from the buffer memory 9 in the data write mode and then supplies them to the head circuit 3 as data to be recorded. In the data read mode, on the other hand, it receives the data from the head circuit 3 and then supplies them to the buffer memory 9 as the read data. In accordance with the present invention, the format control unit 7 generates a jump back signal 72 by itself, and the jump back signal 72 is in turn supplied directly to the servo controller 5 without intervene of the system controller 11 and the drive controller 6.

Turning to Fig. 2, the format control unit 7 includes a decoder 2 decoding or demodulating serial data 7021 which are supplied from the head circuit 3 as data recorded on the disk 1. The data derived from the decoder 702 is converted into parallel data by a serial-parallel/parallel-serial conversion circuit 703. The serial data are further supplied to a synchronizing pattern detector 704. This

detector 704 detects predetermined patterns such as a sector mark indicative of the leading of a sector, an address mark indicative of the beginning of ID information and a data mark indicative of the beginning of data and supplies these detection information to a sequence controller 710 via a bus 7041 to synchronize the controller 710. When ID information indicative of a current sector is obtained in the conversion circuit 703, it is transferred to a current ID register 705. The read-out data obtained in the circuit 703 in the data read mode is transferred to the buffer memory 9 via the bus 12. In the data write mode, on the other hand, the write data from the buffer memory 9 is transferred to the conversion circuit 703 and then converted into serial data which are in turn encoded or modulated by an encoder 701. Serial data 7011 to be recorded on the disk 1 are thus obtained and supplied to the head circuit 3.

ID information stored in the current ID register 705 is changed each time an accessible sector is changed. The ID information is compared by a comparator 706 with an output of a selector 707. This selector 707 selects and outputs the content of a target ID register 708 when a selection signal 7071 is at the low level. On the other hand, the high level of the signal 7071 causes the selector 707 to select and output the content of a suspended ID register 709. The target ID register 708 is loaded by the system controller 11 with ID information indicative of a sector from which data read/write operation starts. The suspended ID register 709 captures the content of the current ID register 705 in response to an ID fetch signal 7091.

The output 7061 of the comparator 706 is supplied to the sequence controller 710 which also receives a read ready signal 1021 and a write ready signal 1022 as data ready information 102 from the memory control unit 10. The sequence controller 710 responds to the synchronizing information 7041, the comparison output signal 7061, data ready information 102 and command information from the controller 11 and generates a set of sequence control signals 7101 for performing a sequence of operations. The sequence control signals 7101 contain the selection signal 7071 and ID fetch signal 7091. The controller 710 further generates the jump back signal 72 which is in turn supplied directly to the servo controller 5.

Referring to Fig. 3, there is shown a tracking servo loop circuit and a jump back control circuit in the servo controller 5 and a part of the optical head circuit 3. A laser beam 31 from a laser diode 305 as an optical source is applied to the disk 1 through a beam splitter 303 and a lens 301. The laser beam reflected from the disk 1 is supplied to a read-out control circuit 304 by the beam spritter 303. The circuit 304 produces the serial data 7021 to be supplied to the format control unit 17. The circuit 304 further produces tracking information of the beam 31 and supplies it to a tracking error producing circuit 305 in which tracking error information is produced and then supplied through a phase compensation circuit 306, a selector 307 and a driver 308 to a tracking actuator 302 to carry out a tracking control. The circuit 306 compensates the phase delay of the actuator 302. The serial data 7011 to be recorded is supplied to a recording control circuit 306 to drive the laser diode 305.

The selector 307 receives the tracking error compensation signal from the circuit 306, a jump back drive signal 721 from a jump back circuit 720 and a seek drive signal 611 from the drive controller 6 and selects and outputs one of them in response to the levels of a jump back instruction signal 722 and a seek instruction signal 612. Specifically, when only the signal 722 takes the active level, the jump back drive signal 721 is selected and outputted. The seek drive signal 611 is selected when the signal 612 is at the active level. When both the signals 612 and 722 are at the inactive level, the tracking error compensation signal is selected.

The jump back circuit 720 includes two S-R type flip-flops 310 and 311, a NAND gate 312, an AND gate 313, a P-channel transistor 314, an N-channel transistor 315, a delay circuit 309 and a tracking cross detector 308 which are connected as shown. Accordingly, the jump back signal 72 from the sequence controller 710 of the format control unit 7 sets both flip-flops 310 and 311 to chance the signal 722 to the active level and turn the transistor 134 ON. The tracking servo loop is thereby made open. The actuator 302 is driven by the V_{DD} level, so that the laser beam 31 starts to move back to a track that is just before the current track. When the laser beam 31 crosses an intermediate point between two tracks, the detector 308 produces the detection output to reset the flip-flop 311. The transistor 314 is thereby turned OFF, whereas the transistor 315 is turned ON to brake the lens 301. The output of the detector 308 is delayed by a predetermined time by the delay circuit 309, and the delayed output resets the flip-flop 310. As a result, the tracking servo loop is formed again. The one-track jump back operation is thus completed.

An operation will be described below with reference to Figs. 1 to 3 and further to Fig. 4 illustrating the track configuration on the disk 1. When the host processor 14 issues data read/write command, the system controller 11 responds to command and produces and stores into the target ID register 708 ID information indicative of the physical address of a sector from which the data read/write operation starts, denoted by a read/write com-

mencement sector 101 in Fig. 4. The system controller 11 further requests the sequence controller 710 to initiate a sequence flow for data read or write and supplies the drive controller 6 with seek information for roving the laser beam 31 to the neighborhood of the read/write commencement sector 101 by the seek operation. In response thereto, the drive controller 6 produces the seek drive signal 611 with making the signal 612 active, so that the laser beam 31 moves to the neighborhood of the sector 101. The signal 612 is thereafter changed to the inactive level to activate the tracking servo loop. The serial data 7021 from the readout control circuit 304 are thereby supplied to the decoder 702 and the synchronizing pattern detector 704. As described above, ID information to be stored in the current ID register 105 is changed each time the accessible sector varies. Since the selection signal 7071 is at the low level in an initial state, the content of the target ID register 708, i.e. the ID information of the data read/write commencement sector 101, is compared by the comparator 706 with the content of the current ID register 705.

When the comparator 706 produces the active level signal 7061 to inform that the read/write commencement sector 101 is accessible, the sequence controller 710 checkes the level of data ready information 102 before requesting the memory control unit 10 to transfer data between the buffer memory 9 and the conversion circuit 703. The write ready signal 1022 of the data ready information 102 is in the active level when write data is stored in the buffer memory 9 in the data write mode, and the read ready signal 1021 thereof is in the active level when the buffer memory 9 has a vacancy for accepting the read-out data in the data read mode. The sequence controller 710 monitors the ready signal 1021 or 1022 in accordance with the operation mode to be executed. When the monitored ready signal 1021 or 1022 is in the inactive level at a time the comparison output signal 7061 becomes active, the data read/write cannot be performed. Therefore, the sequence controller 710 generates the jump back signal 72. Consequently, as already described with reference to Fig. 3, the laser beam 31 jumps back to a track 105 that is just before a track 104 on which the read/write commencement sector 101 exists.

The sequence controller 710 further generates the ID fetch signal 7091, so that ID information of the read/write commencement sector 101 is stored in the suspended ID register 709 as a read/write-suspended sector information. The selection signal 7071 is thereafter changed to the high level to cause the selector 707 to select the register 709.

When the laser beam 31 shifts from the track 105 to the track 104 by the rotation of the disk 1 and the ID information of the sector 101 is then stored in the current ID register 705, the comparator 706 generates again the active level output signal 7061. Assuming that the write data is stored in the buffer memory 9 from the host processor 14 or the buffer memory 9 has a vacancy for accepting the read data before the active level signal 7061 is generated again, the monitored ready signal 1021 or 1022 is at the active level at a time the signal 7061 becomes active. Accordingly, the sequence controller 710 requests the data transfer of the memory control unit 10. In the data write mode, the write data is thereby transferred from the buffer memory 9 to the conversion circuit 703. In the data read mode, on the other hand, the read data is transferred from the conversion circuit 703 to the buffer memory 9.

If the monitored ready signal 1021 or 1022 is still at the inactive level when the signal 7061 comes active again, the jump back operation is repeated.

After the data read/write operation starts from the sector 101, the sequence controller 710 checks the monitored ready signal 1021 or 1022 irrespective of the level of the comparison signal 7061 each time the content of the current ID register 705 changes.

As denoted by a suspended sector 102 in Fig. 4, assume that the mentioned ready signal 1021 or 1022 is at the inactive level when the ID information indicative of the sector 102 is stored in the current ID register 705. The sequence controller 710 therefore generates the jump back signal 72 to back the track to be accessed by one. The ID information of the sector 102 is stored into the suspended ID register 709. After the jump back operation is completed, the content of the current ID register 705 changes in sequence. When the current ID register 705 stores the ID information indicative of the suspended sector 102, the comparison output signal 7061 becomes active. In response thereto, the sequence controller 710 requests again the jump back operation or requests the data transfer for the sector 102 in accordance with the monitored ready signal 1021 or 1022.

After the data read/write operation for the sector 102 is completed, the sequence controller 710 checks the ready signal 1021 or 1022 irrespective of the comparison output signal 7061 each time the content of the current ID register changes, as described hereinbefore.

Thus, the format control unit 7 detects whether or not the data read/write for the currently accessible sector is performed and then generates by itself the jump back signal 72 when the data read/write is disable. The jump back signal 72 controls directly the jump back circuit 720 to perform one-track jump back operation. Therefore, the

access time is free from delay due to the response time of the system controller 11 and the drive controller 6. Moreover, the processing load of the system controller 6 is reduced.

The disk controller is required to execute a write-verify operation in which data from the host processor are recorded on the disk and thereafter the recorded data is read out and checked whether or not any error is contained. This operation is executed in general as follows.

That is, the format control unit informs the system controller of the completion of data recording. In response thereto, the system controller requests the seek operation of the drive controller to back the optical beam by a predetermined number of tracks. Thereafter, the format control unit receives a verifying command from the system control.

In such an operation, as shown in Fig. 4, if the data write commencement sector 101 is close to a data write end sector 103, while it is sufficient to back the beam 31 by two tracks, due to the delay of response time of the controllers 11 and 6, the beam 31 has already passed the write commencement sector 101 at the time the beam 31 is backed by two tracks. For this reason, the beam 31 requires to be backed by three tracks, resulting in that the initiation of the verifying operation is delayed.

A circuit construction for solving the above problem is shown in Figs. 5 and 6 as another embodiment of the present invention, in which the same constituent as those shown in Figs. 2 and 3 are denoted by the same reference numerals to omit further description thereof.

The format control unit according to the present embodiment further includes an S-R type flip-flop 750, an AND gate 751, a down counter 752 and a sector register 753, and a track register 754 is provided in the sequence controller 710. The sector register 753 is loaded with the number of sectors to be subjected to data recording from the system controller 11. The track register 754 is loaded with the number of tracks to be backed ("2" in the example shown in Fig. 2) from the system controller 11.

The jump back operation which may be performed in the data write mode responsive to the write-verify operation is omitted because it is the same as the former embodiment.

By the generation of the comparison output signal 7061 due to the write commencement sector 101 becoming accessible, the flip-flop 750 is set to open the AND gate 751 and the content of the sector register 753 is loaded to the down counter 752. The sequence controller generates a count signal 7511 every time the write data is recorded on the sector, so that the content of the down counter 752 is decremented one by one. When the count value reaches zero, i.e. when the data write operation to the write end sector 103 is completed, the sequence controller 710 outputs the content of the track register 754 onto the data line 541 and thereafter generates the jump back signal 72.

Turning to Fig. 6, the jump back circuit 720 according to the present embodiment further includes a down counter 760, a zero detector 761, an AND gate 762 and an OR gate 763. The data on the line 541 is loaded to the down counter 760. By the jump back signal 72 being thereafter generated, one-track jump back operation is executed and the content of the down counter 760 is decremented by one. The signal from the delay circuit 309 representative of the completion of one-track jump back operation passes through the AND gate 762 and then sets the flip-flops 310 and 311 as the jump back signal. The one-track jump back operation is thereby performed again. Since the content of the down counter 760 reaches zero, the detector 761 closes the AND gate 762. The output from the delay circuit 309 is thereby masked. Thus, the jump back operation for backing the beam 31 by two tracks is performed immediately. The comparator 706 thereafter generates the active level output signal 7061 for initiating the verifying operation.

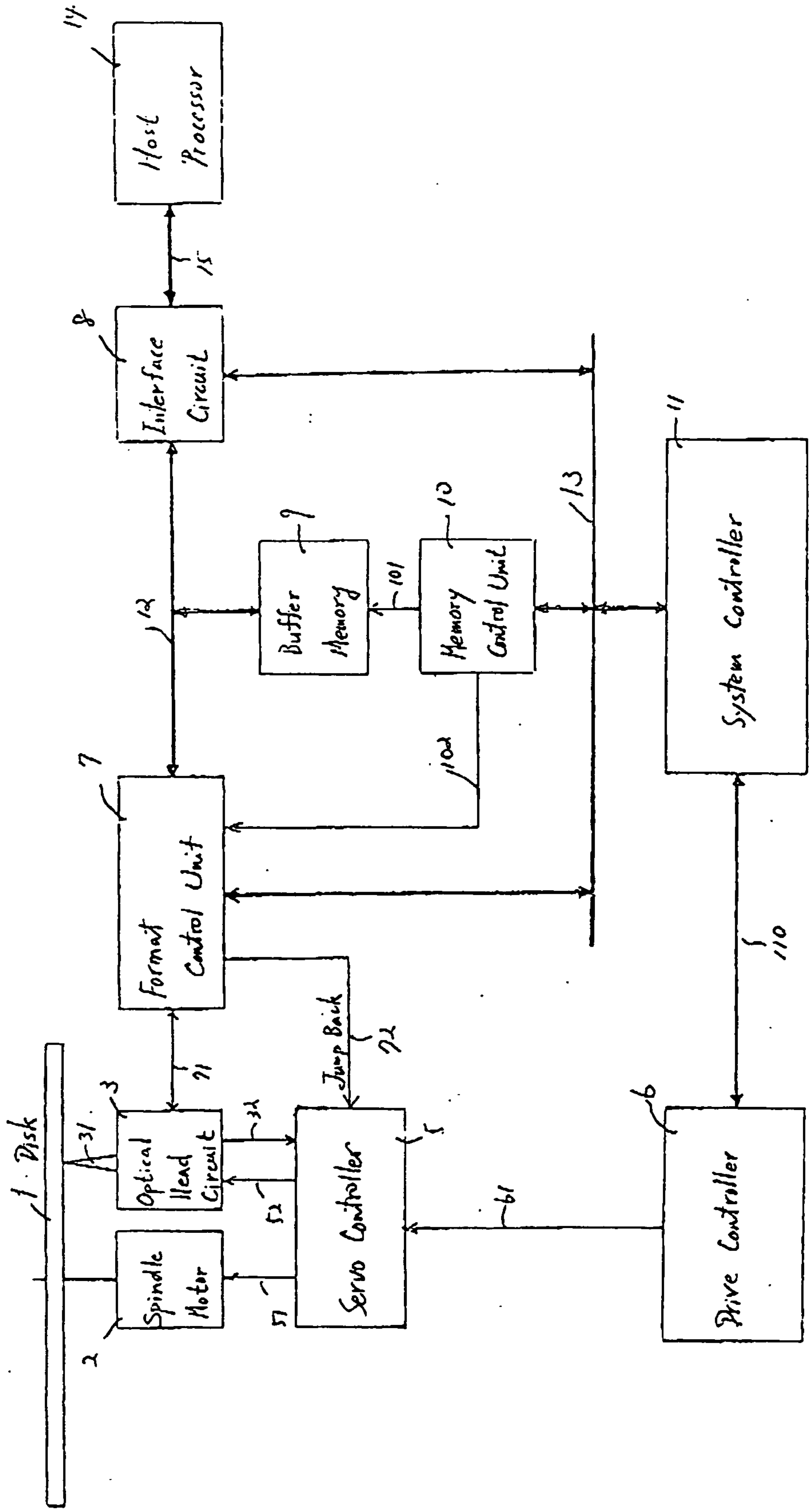
It is apparent that the present invention is not limited to the above embodiments but may be modified and changed without departing from the scope and spirit of the invention. For example, in place of the selector 707, two comparators can be provided, one of which compares the current ID register with the target ID register and the other of which compares the current ID register with the suspended ID register, one of outputs of these comparator being selected. Moreover, a part of the buffer memory can be provided in the format control unit.

Claims

1. A disk controller for a disk having spirally formed tracks, comprising a buffer memory for temporarily storing write data to be recorded on said disk and read data derived from said disk, a first register for temporarily storing current sector information representative of a sector currently accessible, said current sector information being changed in accordance with rotation of said disk, a second register for temporarily storing target sector information representative of a sector from which a data read/write operation starts, comparator means for comparing said current sector information with said target sector information to produce a comparison output signal taking an active level

when said current sector information coincides with said target sector information, means for producing a ready signal taking an active level when said write data is stored in said buffer memory or when said buffer memory has a vacancy for accepting said read data, and control means responsive to said comparison output signal and said ready signal for generating a jump back signal when said ready signal is at an inactive level at a time when said comparison output signal takes said active level, said control means further generating, after said comparison signal takes said active level, said jump back signal when said ready signal is at said inactive level at a time then said current sector information changes.

2. The disk controller as claimed in claim 1, further comprising a third register for retaining the current sector information of said first register at a time when said jump back signal is generated and means for generating a coincident signal when the contents of said first and third registers become equal to each other, said control means generating said jump back signal again when said ready signal is at said inactive level at a time when said coincident signal is generated.



Host Processor
14
15
Interface Circuit
8
13
System Controller
11
Buffer Memory
9
101
Memory Control Unit
10
12
102
Format Control Unit
7
Jump Back
72
71
110
1 Disk
31
3
32
Optical Head Circuit
Servo Controller
5
52
61
Drive Controller
6
Spindle Motor
2
51

Fig. 1

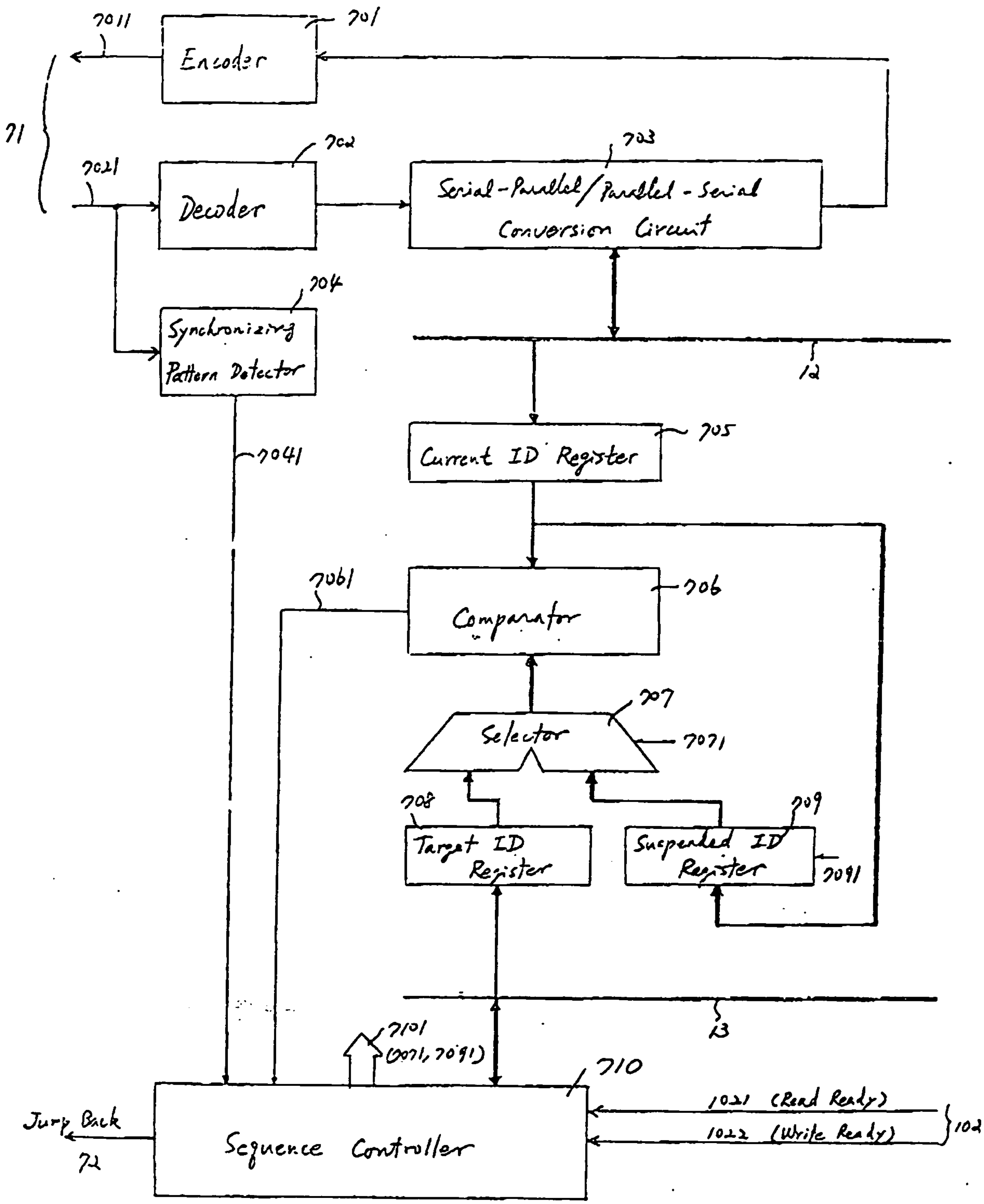

7011
701
Encoder
71
702
703
7021
Decoder
Serial-Parallel/Parallel-Serial Conversion Circuit
704
Synchronizing Pattern Detector
12
705
7041
Current ID Register
7061
706
Comparator
707
Selector
7071
708
709
Target ID Register
Suspended ID Register
7091
13
7101 (7071, 7091)
710
1021 (Read Ready)
1022 (Write Ready)
102
Jump Back
72
Sequence Controller

Fig. 2

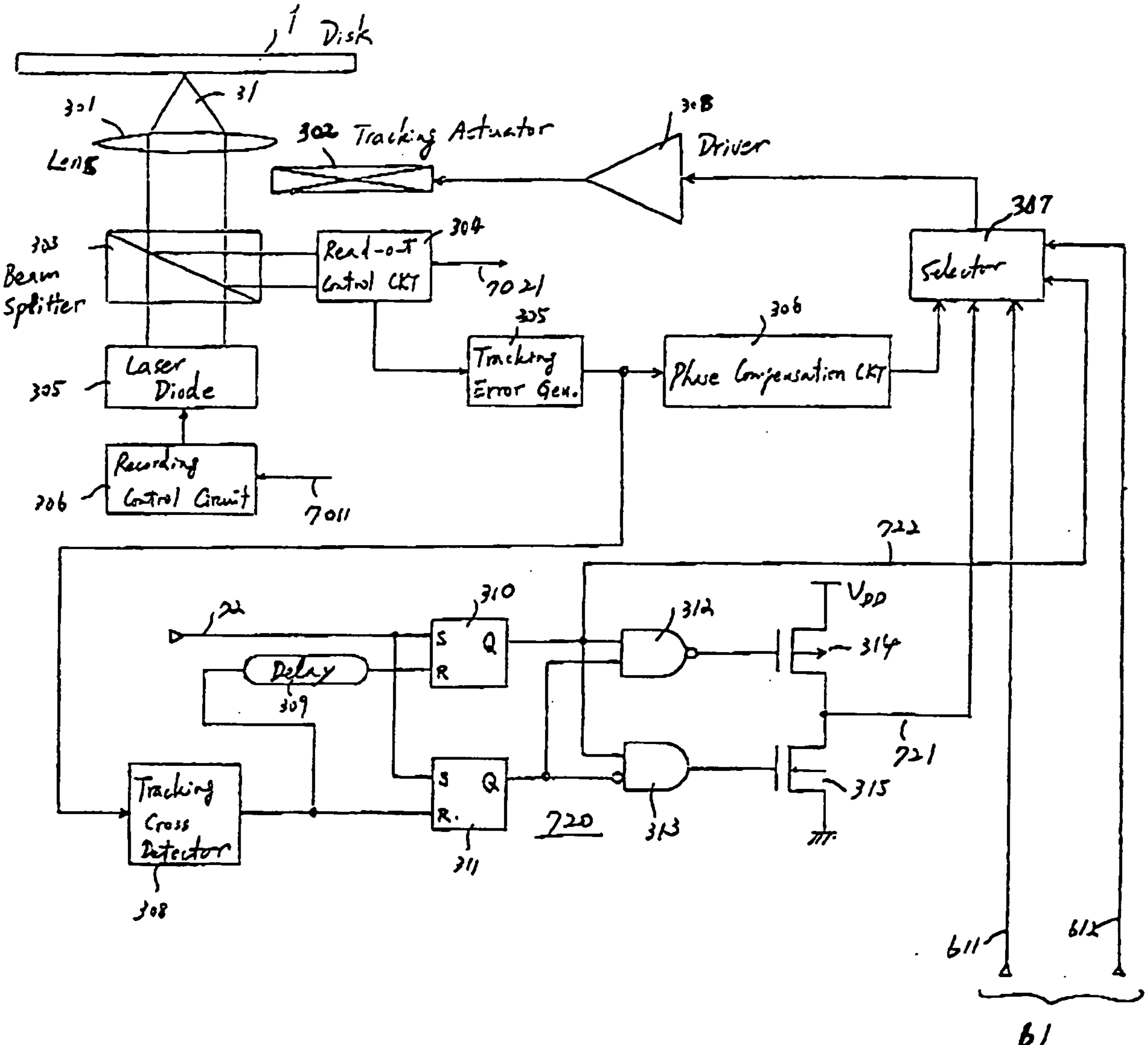

1 Disk
31
301
Lens
302 Tracking Actuator
308
Driver
303
Beam Splitter
Read-out Control CKT
304
7021
305
Tracking Error Gen.
306
Phase Compensation CKT
307
Selector
305
Laser Diode
Recording Control Circuit
306
7011
722
VDD
22
310
S Q
R
312
314
Delay
309
721
Tracking Cross Detector
S Q
R.
720
313
315
311
308
611
612
61

Fig. 3

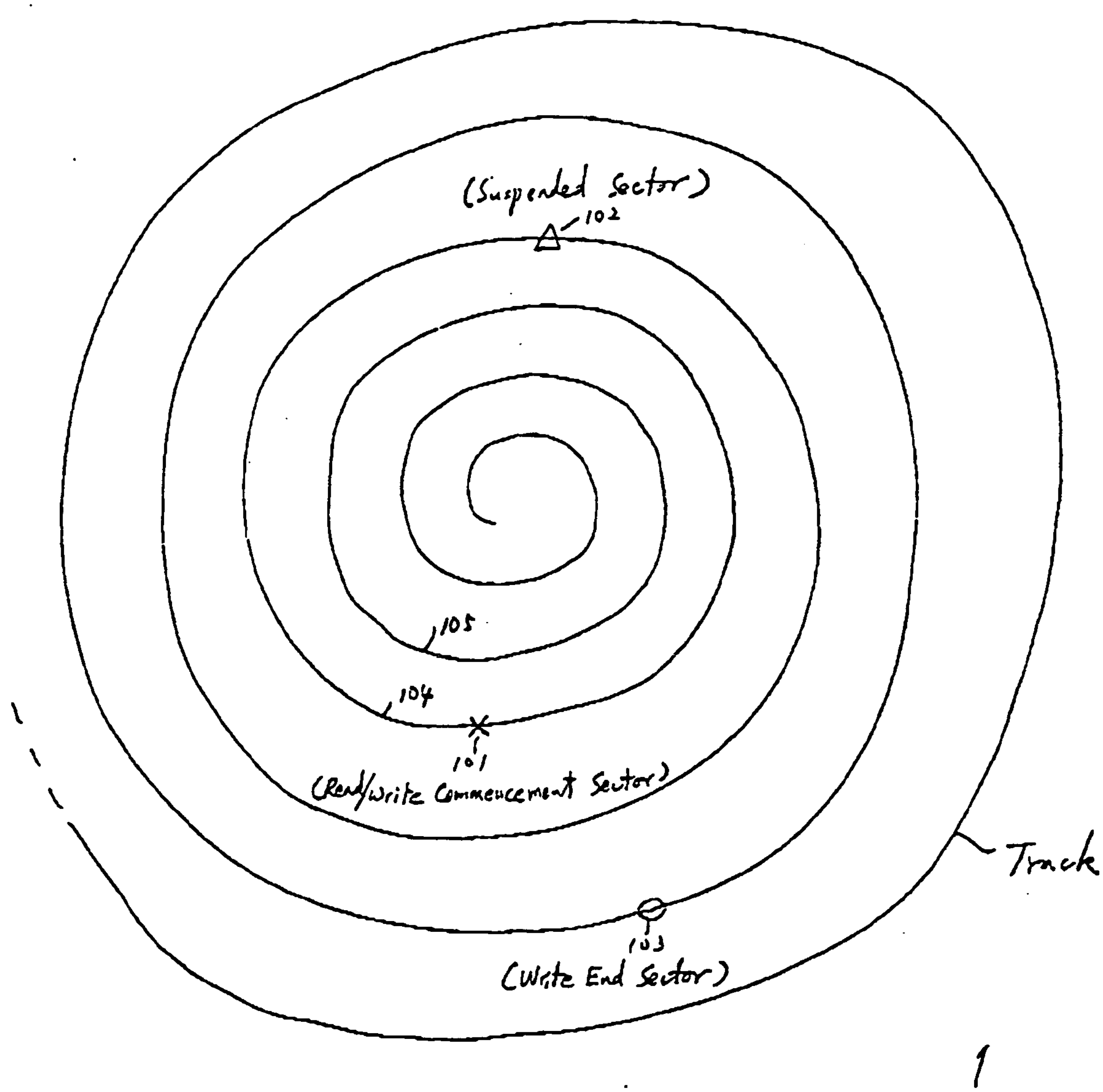

(Suspended Sector)
102
105
104
101
(Read/write Commencement Sector)
Track
103
(Write End Sector)
1

Fig. 4

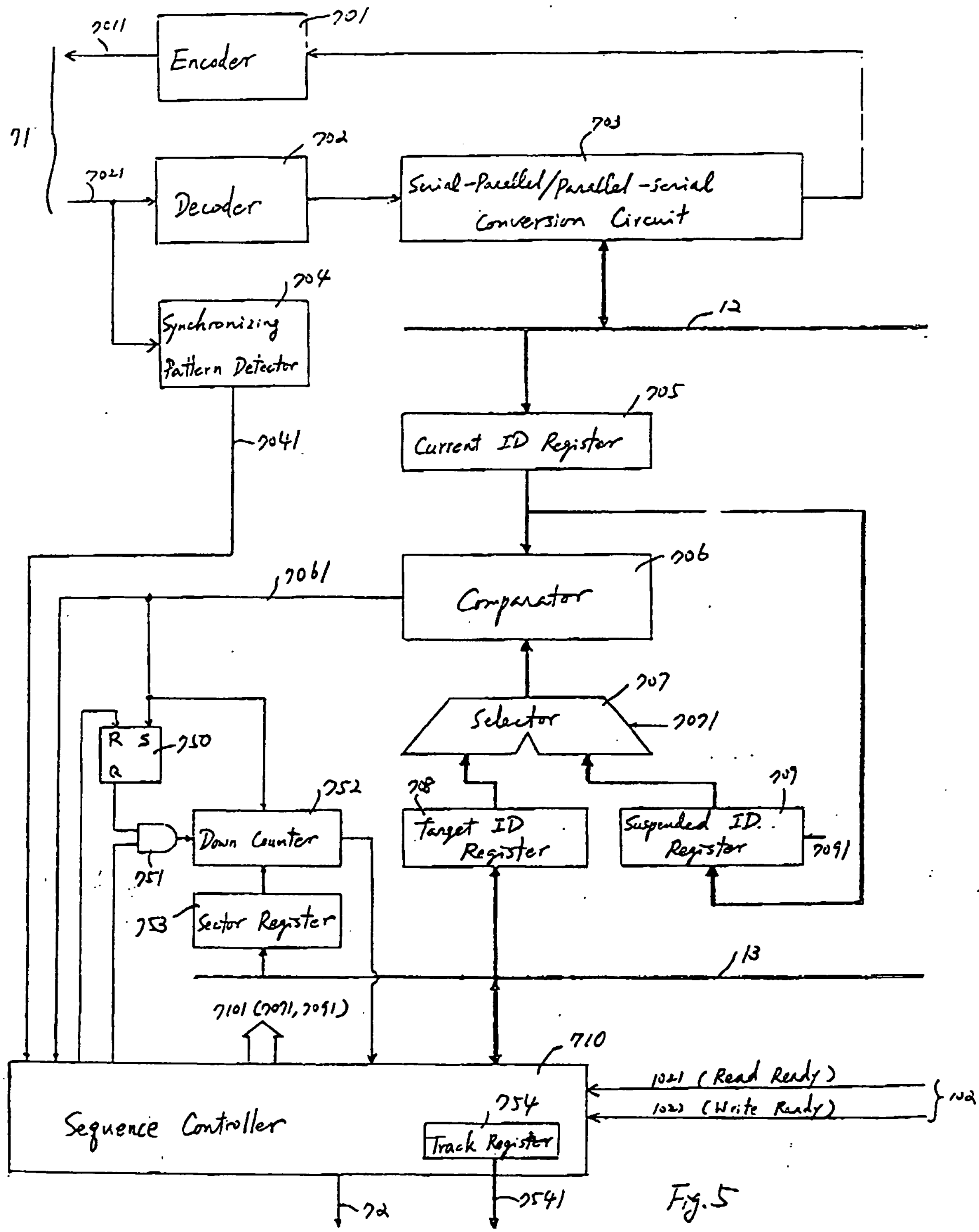

7011
701
Encoder
71
703
702
7021
Decoder
Serial-Parallel/Parallel-serial Conversion Circuit
704
12
Synchronizing Pattern Detector
705
7041
Current ID Register
706
7061
Comparator
707
Selector
7071
R S
Q
750
752
708
709
Down Counter
Target ID Register
Suspended ID. Register
7091
751
753
Sector Register
13
7101 (7071, 7091)
710
1021 (Read Ready)
1022 (Write Ready)
102
754
Sequence Controller
Track Register
72
7541

Fig.5

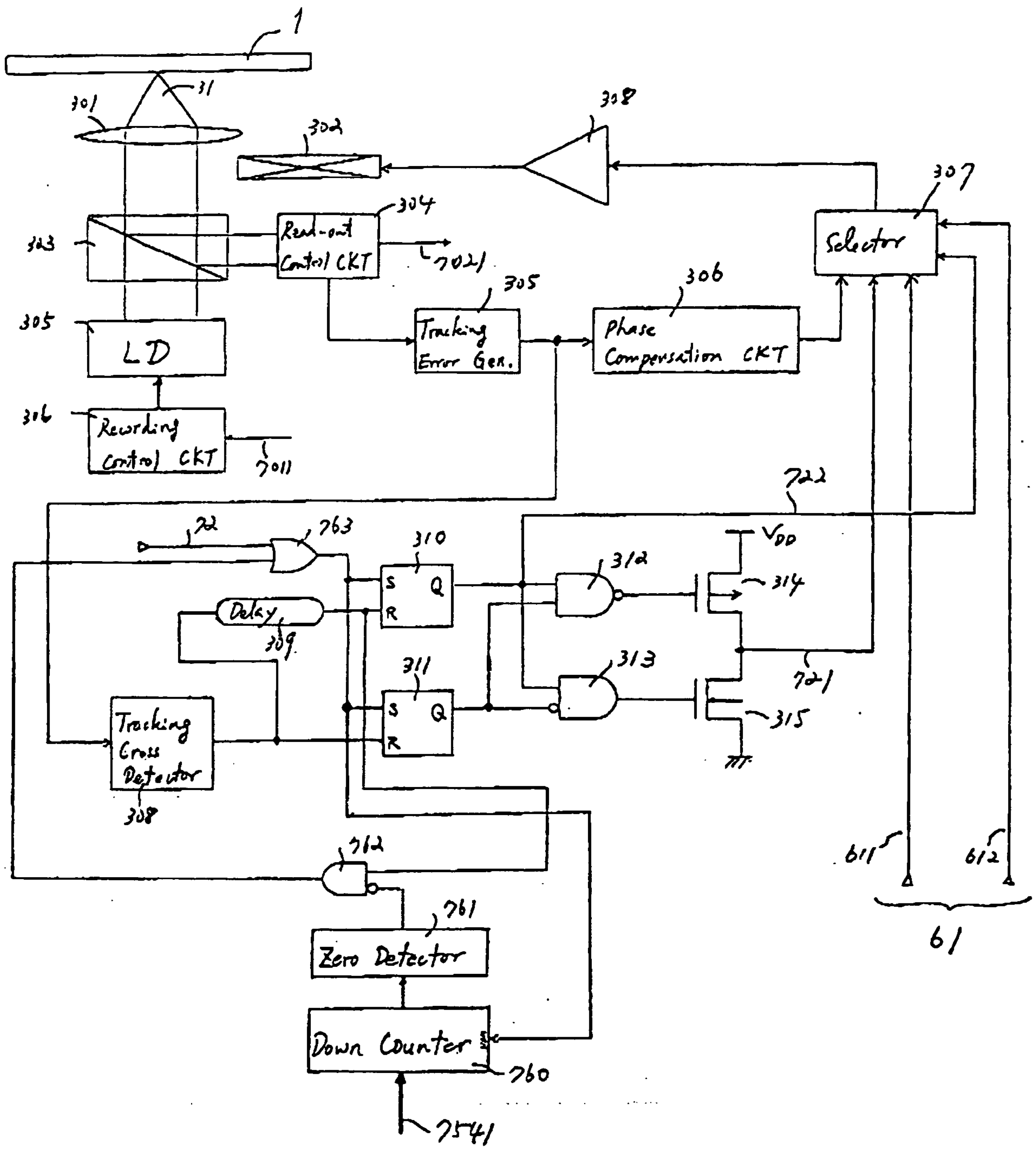

1
31
301
302
308
307
303
Read-out Control CKT
304
7021
305
Tracking Error Gen.
306
Phase Compensation CKT
Selector
305
LD
306
Recording Control CKT
7011
722
72
763
310
Vpp
312
S
Q
R
314
Delay
309
721
311
313
S
Q
R
315
Tracking Cross Detector
308
611
612
712
61
761
Zero Detector
Down Counter
760
7541

Fig. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 91112804.9

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP - A2 - 0 352 131 (SHARP K.K.) * Fig. 1,2; column 1, line 3 - column 4, line 19 * --	1	G 11 B 7/085 G 11 B 7/08 G 11 B 7/09
A	EP - A2 - 0 367 094 (TOSHIBA K.K.) * Fig. 1,2; abstract * --	1	
A	EP - A2 - 0 378 394 (SHARP K.K.) * Fig. 1,4; abstract; column 4, line 17 - column 7, line 28 * ----	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G 11 B 7/00 G 11 B 21/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	11-10-1991	BERGER

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document